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PHILIPS

ADDRESS AND DATA BUS

INTERFACING TECHNIQUES MP53

AN APPLICATION MEMO

signetics

1. INTRODUCTION

The Signetics 2650 Microprocessor has a 15-bit address bus and an 8-bit bi-directional data bus. The address bus allows a maximum of 32K words of memory. The drive capability of the 2650 address and data busses limits the number of chips that can be connected to the system. If the system load exceeds the 2650 drive capability, buffer circuits must be added.

This applications memo provides several examples of interfacing the 2650 address and data busses with ROMs and RAMs such as the 2608, 2606, and 2602. Examples are included for both small and large systems.

2. SMALL SYSTEMS WITHOUT BUFFERING

Address Bus Loading

All 2650 output signals are TTL-compatible. Each output can source 100 μA at 2.4V minimum and sink 1.6 mA at 0.45V maximum. The 2650 inputs require a load current of only 10 μA regardless of the logic level on the input.

The 2608, 2606, 2604, and 2602 MOS ROMs and RAMs all require an input current of 10 μA . This means that, based on d-c loading considerations, a maximum of ten inputs of this type can be driven from one 2650 address output without the use of buffering.

TABLE I
TYPICAL 2650 MEMORY CONFIGURATIONS WITHOUT BUFFERING

Number of Chips Connected to One Address Output	Memory Capacity
Eight 2606 RAMs (256 x 4) Two 2608 ROMs (1024 x 8)	1K byte RAM; 2K bytes ROM
Eight 2602 RAMs (1024 x 1) Two 2608 ROMs (1024 x 8)	1K byte RAM; 2K bytes ROM

If bipolar PROMs such as the 82S114 or 82S115 are used, fewer chips can be connected because of higher input current requirements.

Data Bus Loading with the 2606 RAM (256 x 4)

The bi-directional data bus of the 2606 RAM (256 x 4) makes this device ideally suited for use with the 2650 Microprocessor. The maximum number of input/output connections can be calculated from the diagram shown in Figure 1.

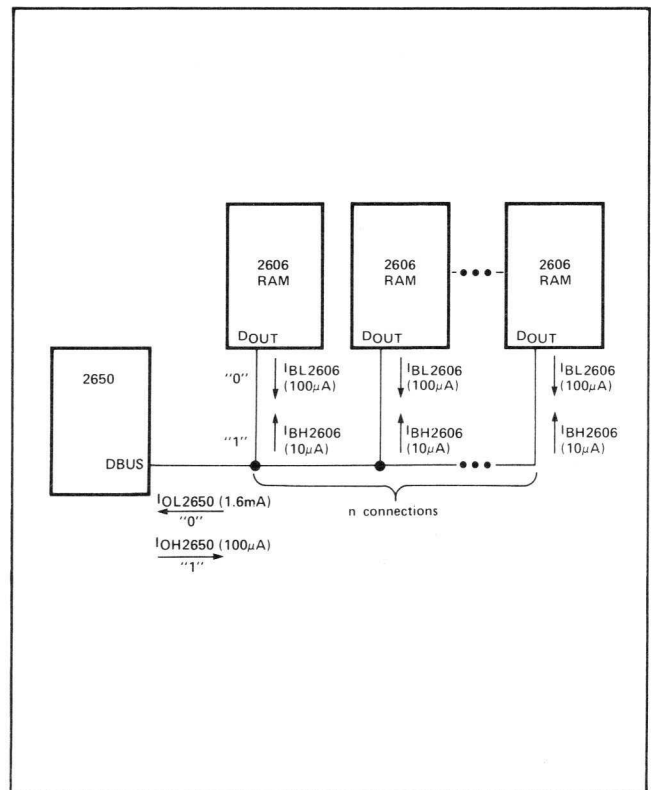


FIGURE 1 The 2606 RAM with the 2650

In Figure 1, n 2606 memory chips are driven by the 2650. The 2606 memory chips load the bus with a leakage current of 100 μA in the logic ZERO state and with 10 μA in the logic ONE state. When the data bus is driven to a logic "1" the required source current of the 2650 output will be:

$$I_{OH2650} = (n) \cdot I_{BH2606}$$

$$= (n) \cdot (10 \mu\text{A})$$

where:

$$I_{BH2606} = \text{output logic ONE leakage current of the 2606 RAM;}$$

and

I_{OH2650} = output logic ONE drive current of the 2650.

From this equation we calculate n_{max} :

$$n_{max} = \frac{I_{OH2650 \max}}{10 \mu A} = \frac{100 \mu A}{10 \mu A} = 10$$

In the logic ZERO state, the output current required of the 2650 is:

$$I_{OL2650} = (n) \cdot I_{BL2606} \\ = (10) \cdot (100 \mu A) = 1000 \mu A$$

where:

I_{BL2606} = output logic ZERO leakage current of the 2606 RAM;

and

I_{OL2650} = output logic ZERO drive current of the 2650.

This is less than the maximum drive capability of 1.6 mA for the 2650.

When the 2606 drives the data bus, the logic ONE loading is the same as that seen by a 2650 driving a data bus (previously described as I_{OH2650}). The logic ZERO load on the 2606 chip is:

$$I_{OL2606} = (n-1) I_{BL2606} + I_{LOL2650} \\ = [(9) \cdot (100 \mu A)] + 10 \mu A \\ = 910 \mu A$$

where:

$I_{LOL2650}$ = output logic ZERO leakage current of the 2650.

This is below the 1.9 mA sink current capability of the 2606. It can thus be concluded that when using MOS RAMs or ROMs with the 2650, the number n is normally limited by the maximum output logic ONE current of the driving device.

Data Bus Loading with the 2602 RAM

In contrast to the 2606, the 2602 RAM (1024 x 1) has separate input and output data paths. The data output for this device is switched to tri-state with the chip enable input. For bi-directional data transfers, however, the data output signal must be disabled during the write mode to avoid a drive conflict between the 2650 and the RAM. This is done by inserting a tri-state buffer into the data-out line as shown in Figure 2. The buffers are only enabled when OPREQ is a "HIGH", \bar{R}/W (the READ/WRITE control line from the 2650) is a "LOW", and the RAM is selected for access.

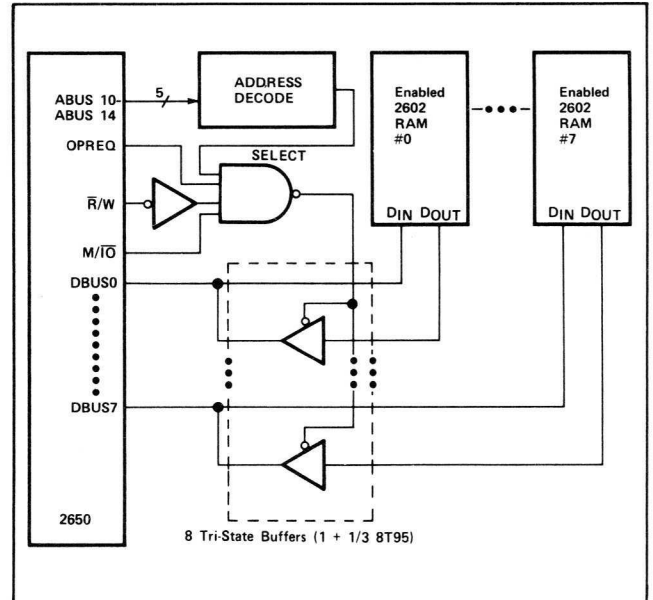


FIGURE 2 The 2602 RAM with the 2650

A-C Loading Considerations

The 2650 address bus, data bus, and control lines will drive a 100 pF capacitive load and one standard TTL load. The capacitive loading calculations must include the 2650 output capacitance and the external wiring capacitance. The 2606 presents a 10 pF capacitive load to the data bus and a 7 pF load to all other inputs. The number (n) of 2606 RAMs that can be driven directly by the 2650 is given by the following equations:

$$C_{LOAD} = C_{OUT2650} + C_{WIRING} + [(n_d) \cdot C_{OUT2606}]$$

or

$$C_{LOAD} = C_{OUT2650} + C_{WIRING} + [(n_a) \cdot C_{IN2606}]$$

where:

- $C_{OUT2650}$ = Output capacitance for the 2650 = 10 pF
- C_{WIRING} = Wiring capacitance = 10 pF
- C_{IN2606} = Load capacitance for the 2606 address bus = 7 pF
- $C_{OUT2606}$ = Load capacitance for the 2606 data bus = 10 pF
- C_{LOAD} = 100 pF

therefore:

$$n_a = \frac{80 \text{ pF}}{7 \text{ pF}} \cong 11 \text{ address bus loads}$$

$$n_d = \frac{80 \text{ pF}}{10 \text{ pF}} \cong 8 \text{ data bus loads}$$

The 2606 is a 256-location by 4-bit RAM and requires two chips for each 256 bytes. As seen from the above calcula-

tions, the 2650 will drive eleven 2606s (n_a), or five pairs ($n_a/2$) of 2606s (1280 bytes) directly. Since this number is less than the number of d-c loads that the 2650 is capable of driving (10), it can be concluded that the a-c loading is the limitation for full-speed operation.

Increasing Fan-Out by Pull-Up Resistor

The fan-out of the 2650 bus in the logic ONE state can be increased with a pull-up resistor. This increases the d-c fan-out of the outputs in the logic ONE state by supplying supplementary drive current. This can be seen from the example shown in Figure 3.

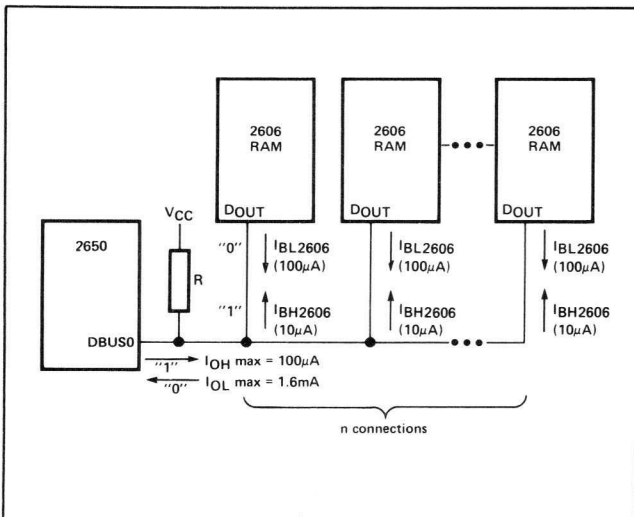


FIGURE 3 Pull-up Resistors for Increased Fan-out

$$\text{Logic ONE state } I_R = \frac{V_{CCmin} - V_{OHmax2650}}{R} = [(n) \cdot I_{BH2606}] - I_{OH2650}$$

$$\text{Logic ZERO state } I_R = \frac{V_{CCmax} - V_{OLmin2650}}{R} = I_{OL2650} - [(n) \cdot I_{BL2606}]$$

where:

$V_{CCmin} = 4.75$ volts
 $V_{CCmax} = 5.25$ volts

$V_{OHmax2650} = 2650$ maximum logic ONE output voltage
 $= V_{CC} - 0.5$ volts
 $V_{OLmin2650} = 2650$ minimum logic ZERO output voltage
 $= 0$ volts

$I_{BH2606} =$ output logic ONE leakage current of the 2606 RAM
 $= 10 \mu A$

$I_{BL2606} =$ output logic ZERO leakage current of the 2606 RAM
 $= 100 \mu A$

$I_{OH2650} =$ output logic ONE current of the 2650
 $= 100 \mu A$

$I_{OL2650} =$ output logic ZERO current of the 2650
 $= 1.6 \text{ mA}$

$n =$ the number of 2606 type loads that can be driven by the 2650

From the above equations, R can be calculated to be 17.5K ohms. The number of 2606 loads (n) is calculated to be 12. Six pairs of 2606 chips can be driven when the pull-ups are added. These calculations are for d-c loading, and the a-c (capacitive) load limitations must still be considered.

With $V_{CCmin} = 4.5V$ and $V_{CCmax} = 5.5V$: $n = 10$
 $R = 9K\Omega$

With $V_{CCmin} = 4.75V$ and $V_{CCmax} = 5.25V$: $n = 12$
 $R = 12K\Omega$

3. LARGE BUFFERED SYSTEMS

In larger microcomputers it is necessary to increase the drive capability of the CPU by adding drivers to the outputs. A generalized 2650 microcomputer system using additional bus drivers is illustrated in Figure 4.

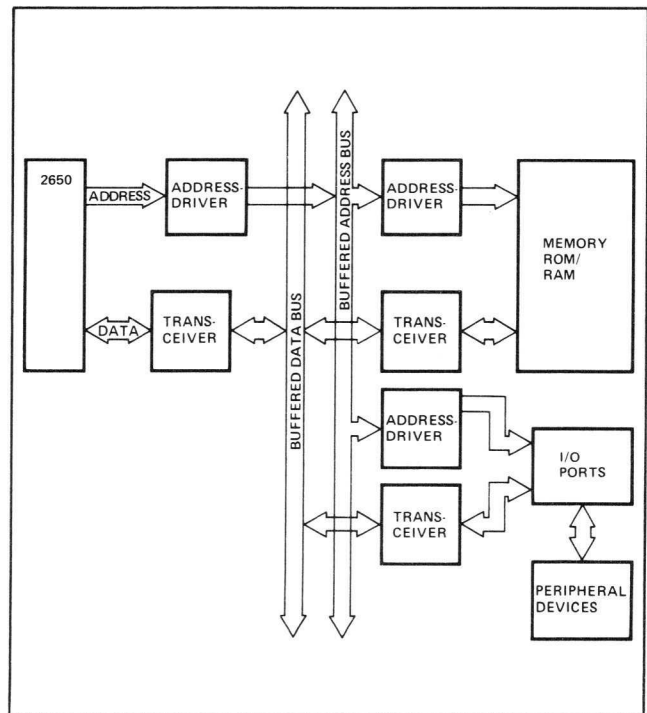


FIGURE 4 General-Purpose Microcomputer System

This system has a buffered address bus and a buffered data bus. To ensure minimal loading, buffers are also included between the memory and I/O ports. With this arrangement, the system can easily be expanded, and each additional device adds a single load to the shared bus.

In some cases, the configuration in Figure 4 can be simplified as shown in Figure 5. The memory and I/O ports are directly driven by the address driver and transceiver circuits.

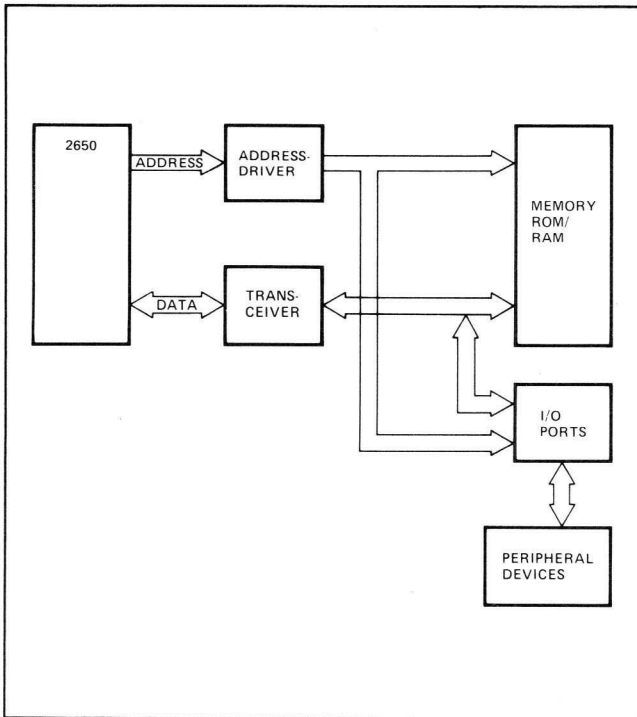


FIGURE 5 Microprocessor with Buffered Address and Data Bus

Address Driver

The address bus driver may be a non-inverting interface element of the 8T family, such as the 8T95 or 8T97 shown in Figure 6.

The tri-state control inputs (DIS4 and DIS2) can be connected to ground if these buffers are always active. For DMA operations, the control inputs can be switched to a HIGH to disconnect the processor from the bus. These Schottky-TTL devices have typical propagation delays of 6 ns. (See Table III.)

Standard TTL buffers may be used to drive the address bus. If buffers with open-collector outputs or tri-state capability are used, DMA operations can be performed.

Data Transceivers

The 2650 bi-directional data lines can be driven with the 8T26 (inverting) and 8T28 (non-inverting) transceivers (Figure 7).

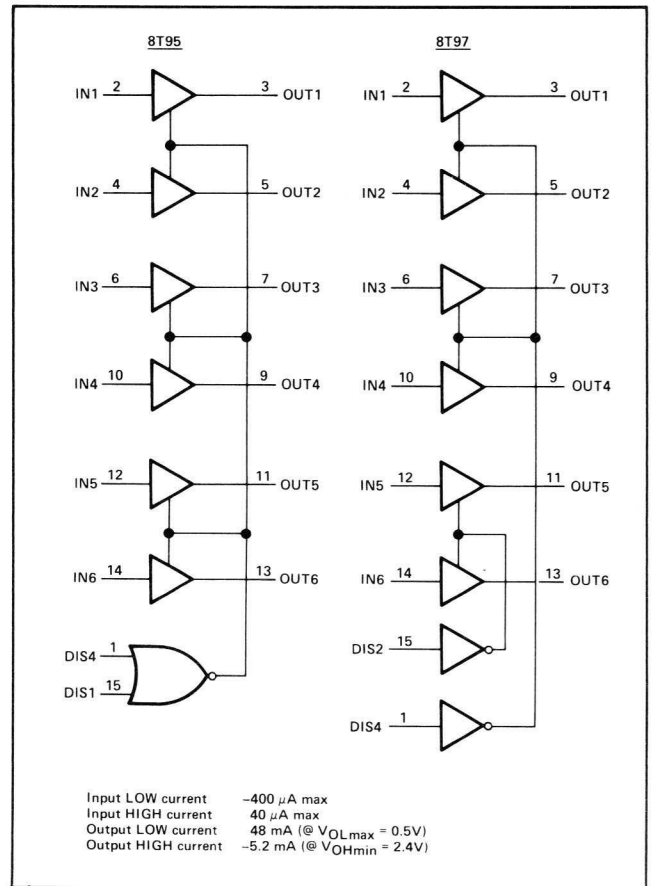


FIGURE 6 8T95 and 8T97 Hex Tri-State Buffers

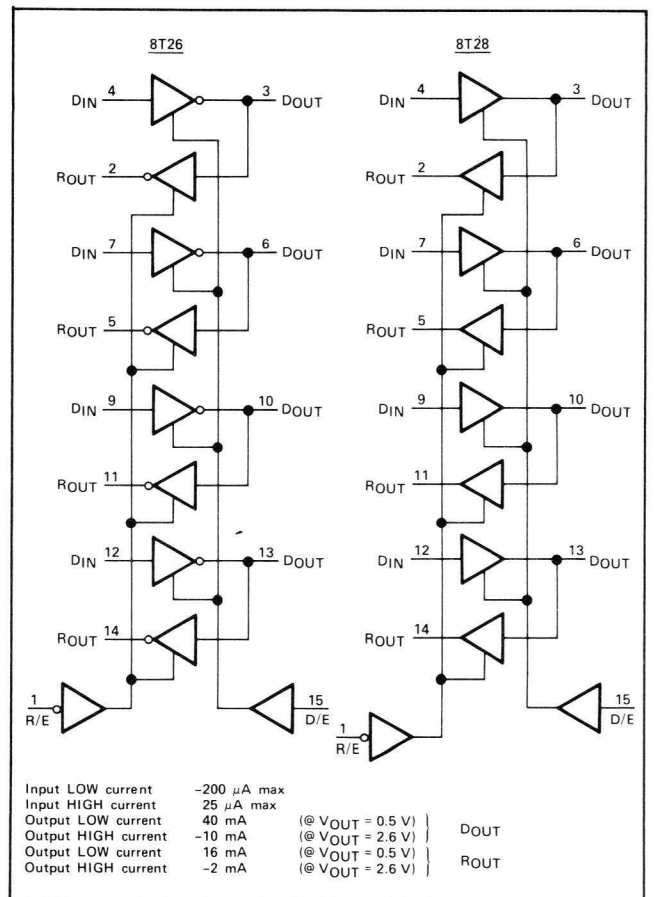


FIGURE 7 Tri-State Quad Bus Transceivers

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The driver can be enabled by the driver enable line (D/E, active high). The receiver can be enabled by the receiver enable line (R/E, active low). To drive the 2650 bi-directional data bus, the DIN and ROUT signals can be tied together to provide a bi-directional data path.

Figure 8 shows a typical application of the transceiver circuit for bi-directional data buffering. The 8T28 features a propagation delay of 20 ns with a 300 pF capacitive load.

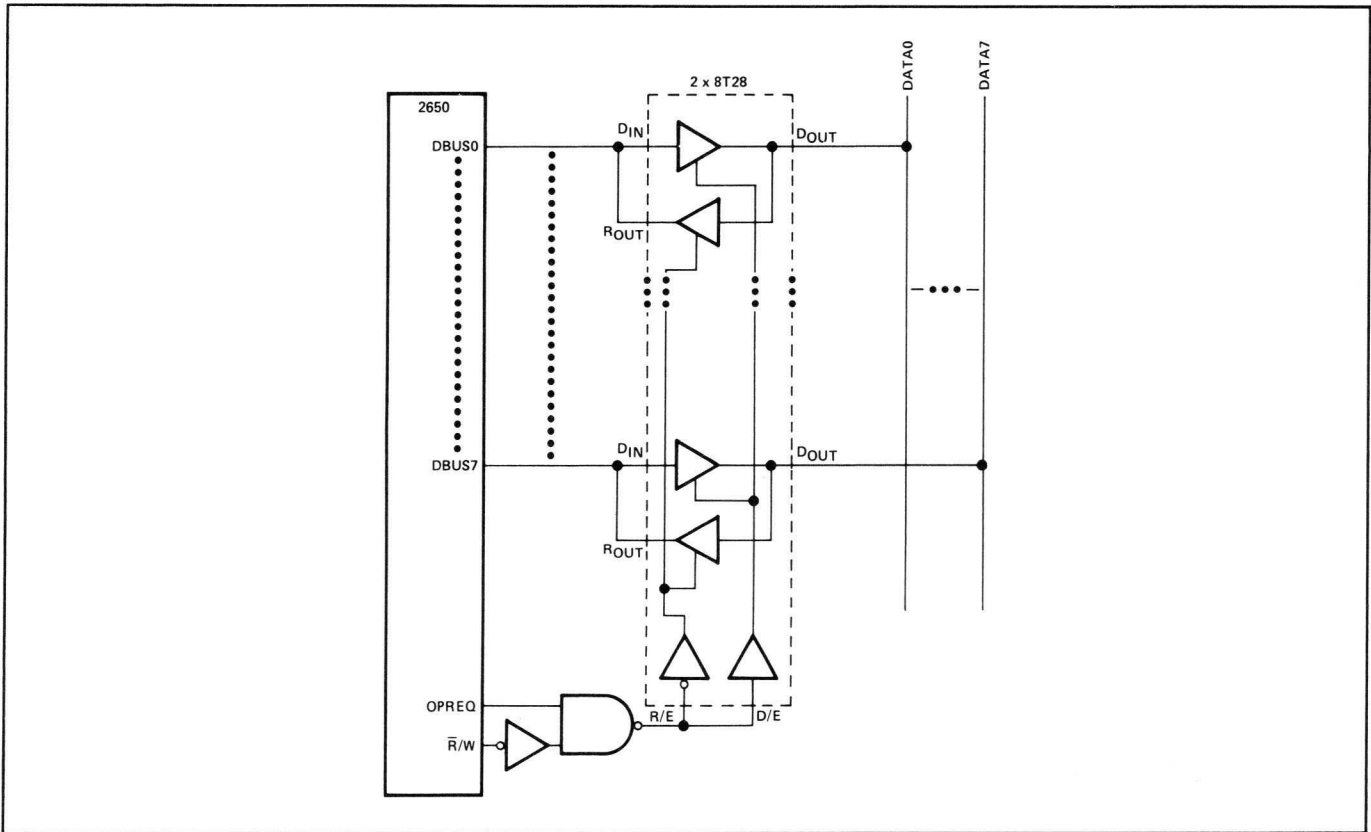


FIGURE 8 Typical Application of the Transceiver Circuit

TABLE II
MOS RAMs - SURVEY OF D-C ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	2606 (256 x 4)	2602 (1024 x 1)	2604 (4096 x 1)	UNIT	TEST CONDITIONS
Maximum input load current	I _{IL}	10	10		μA	V _{IN} = 0 to 5.25V
				10	μA	V _{IN} = +5V
Maximum input LOW voltage	V _{IL}	0.65	0.65	0.6	V	
Minimum input HIGH voltage	V _{IH}	2.2	2.2	2.2	V	
Maximum output LOW voltage	V _{OL}	0.45	0.45		V	I _{OL} = 1.9 mA
				0.4	V	I _{OL} = 3.2 mA
Minimum output HIGH voltage	V _{OH}	2.4	2.4		V	I _{OH} = -100 μA
				2.4	V	I _{OH} = -2 mA
Maximum output HIGH leakage current	I _{BH}	10	10	10*	μA	$\bar{C}E = 2.2V; V_{OUT} = 4.0V$
Maximum output LOW leakage current	I _{BL}	-100	-100		μA	$\bar{C}E = 2.2V; V_{OUT} = 0.45V$
Maximum input capacitance	C _{IN}	7	5	7	pF	V _{IN} = 0V
Maximum bus input capacitance	C _{OUT}	10	10	6	pF	V _{OUT} = 0V
Common I/O		X				
Separate I/O			X	X		

*Test conditions $\bar{C}S = 2.2V; V_{OUT} = 5V$

TABLE III
BUFFERS - SURVEY OF ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	8T09 (quad)	8T95/97 (hex)	8T96/98 (hex)	UNIT	TEST CONDITIONS
Inverting		X		X		
Non-inverting			X			
Maximum input LOW current	I _{ILmax}	-2			mA	V _I = 0.4V; DIS = 0.4V
			-0.4	-0.4	mA	V _I = 0.5V; DIS = 0.5V
Maximum input HIGH current	I _{IHmax}	40			μA	DIS = 4.5V
			40	40	μA	V _I = 2.4V
Maximum input LOW voltage	V _{ILmax}	0.8	0.8	0.8	V	V _{CC} = MIN; T _A = 25°C
Minimum input HIGH voltage	V _{IHmin}	2.0	2.0	2.0	V	V _{CC} = MIN; T _A = 25°C
Maximum output LOW voltage	V _{OLmax}	0.4			V	I _{OL} = 40 mA
			0.5	0.5	V	I _{OL} = 48 mA
Minimum output HIGH voltage	V _{OHmin}	2.4	2.4	2.4	V	I _{OH} = -5.2 mA
Maximum output leakage current HIGH	I _{BH}	40	40	40	μA	V _O = 2.4V
Maximum output leakage current LOW	I _{BL}	-40	-40*	-40*	μA	V _O = 0.4V
Propagation delay (data to output)	t _{ON}	20**	5***	5***	ns	
	t _{OFF}	20	6	6	ns	
Propagation delay (disable to output)	High Z/0	22	12	12	ns	
	High Z/1	22	10	10	ns	

*Test condition V_O = 0.5V

**Test condition C_L = 300 pF

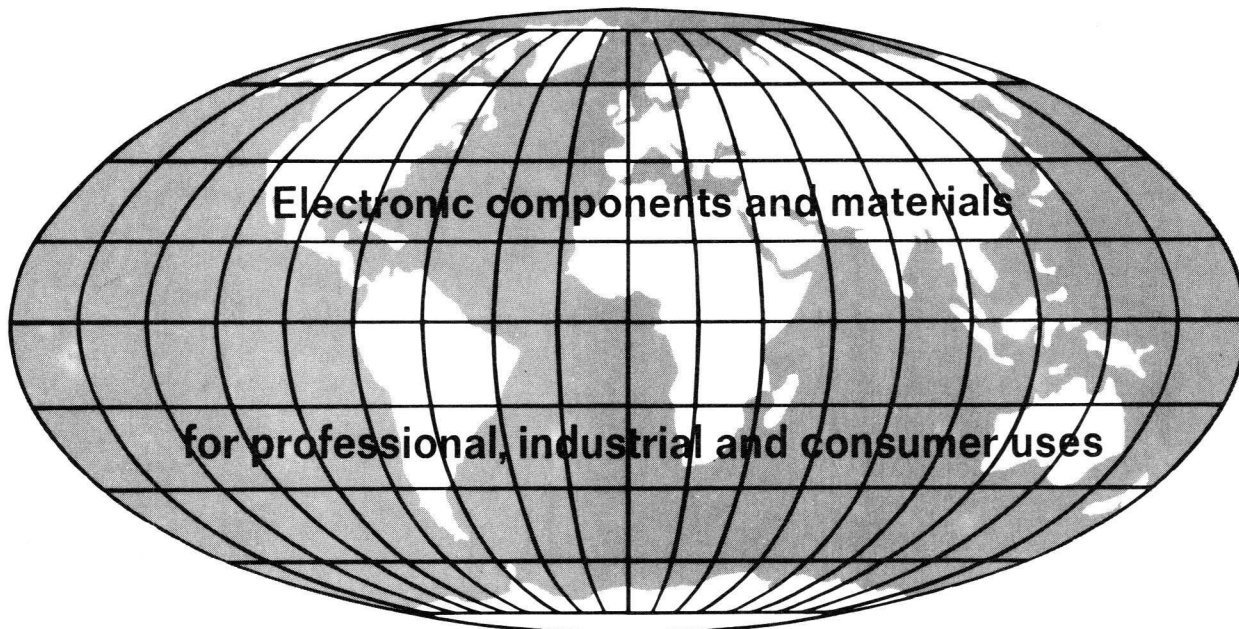
***Test condition C_L = 50 pF

TABLE IV
(P)ROMs - SURVEY OF D-C ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	2608 (1024 x 8)	82S114 (256 x 8) 82S115 (512 x 8)	82S130 (512 x 4) 82S131 (512 x 4)	82S126 (256 x 4) 82S129 (256 x 4)	UNIT	TEST CONDITIONS
Maximum input load current	I _{IL}	10				μA	
Maximum input LOW current	I _{ILmax}	10	-100	-100	-100	μA	V _{IN} = 0.45V
Maximum input HIGH current	I _{IHmax}	10	25	40	40	μA	V _{IN} = 5.5V
Maximum input LOW voltage	V _{ILmax}	0.65	0.85	.85	0.85	V	
Minimum input HIGH voltage	V _{IHmin}	2.2	2.0	2.0	2.0	V	
Maximum output LOW voltage	V _{OLmax}	0.45				V	I _{OL} = 1.6 mA (2608)
			0.5			V	I _{OL} = 9.6 mA (82S114, 82S115)
				0.45	0.5	V	I _{OL} = 16 mA (82S130, 82S131, 82S126, 82S129)
Minimum output HIGH voltage	V _{OHmin}	2.4				V	I _{OH} = -100 μA
			2.7			V	I _{OH} = -2 mA
				2.4	2.4	V	I _{OH} = -2.4 mA
Maximum output leakage current	I _{BH}	10*	40	40	40	μA	V _O = 5.5V; device deselected
Maximum output leakage current L	I _{BL}	-10**	-40	-40	-40	μA	V _O = 0.5V; device deselected
Maximum input capacitance	C _{IN}	7.5	5	5	5	pF	
Maximum output capacitance	C _{OUT}	15	8	8	8	pF	

*Test conditions V_O = 2.4V

**Test conditions V_O = 0.4V



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