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High Quality Preamplifier and Tone Control Circuit Type R105

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This is the first of two articles describing a high quality audio preamplifier and main amplifier. This first article describes the preamplifier which features alternative low noise input circuits for magnetic and ceramic pickup cartridges and a sophisticated type of feedback tone control.

A main amplifier suitable for use with this preamplifier is under development and will be described in a second article which will appear in Radiotronics at a later date. However, the preamplifier appearing in this article may be used with other suitable main amplifiers if desired.

The two input modules to be described in this article have been especially designed in an attempt to reduce noise generated by the transistors themselves, especially flicker noise. At the same time harmonic distortion has been kept at a minimum value.

The circuit shown in fig. 2 is designed as an input stage for a magnetic cartridge. It has a gain of 27 dB at 1 Kc/s and with an input of 5 mV the total harmonic distortion at 1 Kc/s is less than 0.02%. The signal to noise ratio, referred to an input voltage of 5 mV from a 600 ohms source, is better than 65 dB unweighted, or better than 80 dB weighted according to curve A of the A.S.A. Standard S1.4—1961. The use of curve A when measuring signal to noise ratio in audio amplifiers was discussed in an article title "Signal/Noise Measurements in Audio Amplifiers" and published in the September 1964 issue of Radiotronics.

The frequency response of the magnetic input circuit is in accordance with the R.I.A.A. reproduction curve.

Fig. 3 shows a circuit that is designed for use with a ceramic cartridge. It requires an input of 250 mV into 1000 pF capacitor to give an output of 50 mV at 1 Kc/s. The input signal is quoted in this specific manner because the equivalent circuit of a ceramic cartridge consists of a capacitor (approx. 1000 pF) in series with a voltage generator. The signal current supplied to the ceramic input circuit will depend on the signal frequency and the reactance of the 1000 pF capacitor at that frequency.

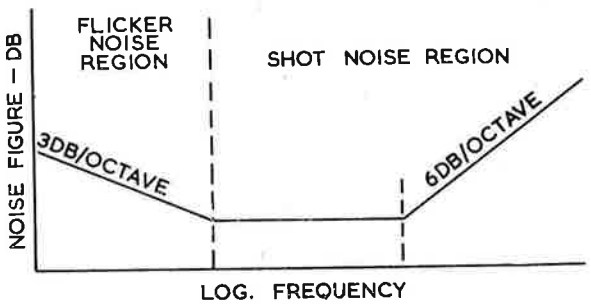
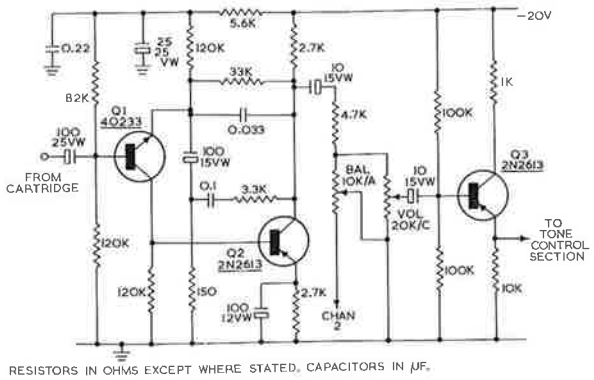


Fig. 1. Diagram of the noise characteristics of a transistor.



RESISTORS IN OHMS EXCEPT WHERE STATED. CAPACITORS IN μF.

Fig. 2. Input stages for magnetic cartridges.

At the above input level the total harmonic distortion is less than 0.04% and the signal to noise ratio is 56 dB weighted (Curve A). The overall frequency response of the module is within 3 dB from 25 c/s to beyond 30 Kc/s.

The tone control circuit, fig. 4, features switched frequency controls for both bass and treble which are operated in conjunction with switched intensity controls. The bass control selects the corner frequency of the lower frequency response in five steps for both boost and cut. The five steps are 1,000, 500, 200, 100 and 50 c/s. The switched treble control selects the upper corner frequencies in four steps for boost and cut. These steps are 1, 2, 5 and 10 Kc/s. The term "corner frequency" in this article refers to the frequency at which the frequency response of the circuit has changed by 3 dB, either in the positive or negative direction.

This means that at any selected corner frequency the response of the amplifier will commence to rise or fall with respect to the "flat" position, depending on whether "boost" or "cut" is selected. This rise or fall will continue at a rate approaching 6 dB per octave, until the maximum value is reached. The maximum value is determined by the intensity switch which has a range from 0 to 21 dB in 3 dB steps.

The complete performance figures of these circuits are listed in table A.

However, before attempting to describe the operation of these circuits, a brief description of

	Magnetic Input Circuit	Ceramic Input Circuit	Tone Control Circuit
Rated Signal Input	5 mV	250 mV into	15 mV
Output	120 mV	0.001 μF	0.65 mA
Harmonic Distortion	<0.01% Total	50 mV	<0.04% Total
Noise (Curve A) . .	>—80 dB	<0.06% Total	—78 dB
Frequency Response		—69 dB	
(—3dB)	RIAA Compensated	26 c/s—40 Kc/s	10 c/s—40 Kc/s (Flat Position)

NOTE: ALL ABOVE MEASUREMENTS AT RATED SIGNAL INPUT.

Table A

the different types of noise in transistors and their causes, will be given. This may be of assistance in understanding the special features of the designs.

NOISE PROBLEM IN TRANSISTORS.

There are three important types of noise generated in semiconductor devices. They are

1. Thermal or Johnson Noise.
2. Shot Noise.
3. Flicker or $\frac{1}{f}$ Noise.

For junction transistors the noise characteristics have the general form shown in fig. 1.

1. Thermal or Johnson Noise. This type of noise is due to the fact that electricity is carried by discrete particles or current carriers (e.g. holes and electrons) which move about within the semiconductor material in a random manner. This random motion of charged particles is due to the resistance of the material and thermal excitation and creates a noise current. Since thermal noise is temperature dependant it may be reduced by operating the device at low temperatures or by reducing the internal resistance of the device.

This means that in a transistor thermal noise is always present and in conventional circuitry it can not be easily reduced.

2. Shot Noise. Shot noise is caused by the fluctuation in the number of current carriers arriving at a point in a semiconductor material. This fluctuation is equivalent to the generation of a moise current within the semiconductor.

In a transistor shot noise arises from fluctuations in the components of the emitter current flowing into the base and the collector. The noise current generated is completely dependant on the current flowing through the device.

3. Flicker or $\frac{1}{f}$ Noise. When transistors are

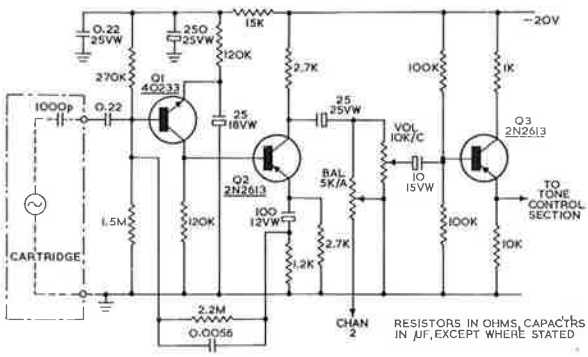


Fig. 3. Input stages for ceramic cartridges.

used in low signal audio circuits flicker noise becomes the most serious of the three types of noise. This is especially so when R.I.A.A. compensation is used in the circuit and boost is applied to the low frequencies.

Flicker noise, due to its $\frac{1}{f}$ characteristic, rapidly increases as the frequency decreases. At very low frequencies and with bass boost applied, flicker noise could cause an amplifier to be driven into overload. To prevent this it may be necessary to restrict the low frequency response of the circuit.

At present flicker noise is not fully understood, but research has shown it may be represented by a current which may be calculated from the expression

$$\bar{i}^2 = \frac{KI}{f} \Delta f \text{ approx.}$$

where $\bar{i}^2$ is the square of the mean value of noise current, K is a constant, I is the D.C. current flowing through the transistor and f is the frequency. From this expression it can be seen that flicker noise is very dependant on the current which flows through the device.

Thus there are two different types of noise generated which are largely dependant on the current which flows through the transistor. To reduce the noise generated it is, therefore, necessary to operate the transistor at a low D.C. collector current. Thermal noise, however, is virtually uncontrollable being dependant on temperature.

CIRCUIT DESCRIPTION.

Magnetic Input Circuit: The first circuit shown (fig. 2) is for use with a magnetic pick-up cartridge and uses three transistors, two A.W.V. 2N2613's and one R.C.A. 40233. The 40233 is a silicon npn planar transistor featuring low noise and low leakage characteristics. A most important point about this transistor, however, is that it has a reasonable h_{fe} at very low collector currents, in the vicinity of 40 to 50 μA.

In the circuit to be described here the collector current of the 40233 (Q1) is approximately 50μA. This current proved to be the best compromise in reducing noise while at the same time keeping the distortion down to a minimum. Q2 (2N2613) is directly coupled to the collector of the 40233 and operates with a collector current of 3 mA approximately.

R.I.A.A. equalisation is provided by frequency selective feedback from the collector of Q2 to the emitter of Q1. It is provided by a 33,000 ohm resistor in parallel with an 0.033 μF and a 3,300 ohm resistor in series with a 0.1 μF capacitor. At 1 Kc/s the amount of feedback present is 28 dB.

The input to the circuit is between the base of Q1 and the positive supply line, which is grounded. The emitter resistor, as far as the input signal is concerned is the 150 ohm resistor from the emitter of Q1 to ground. This avoids the introduction of noise from the supply line.

The low distortion of the module is due mainly to (a) the R.I.A.A. compensation which tends to reduce harmonics and (b) the large amount of feedback present.

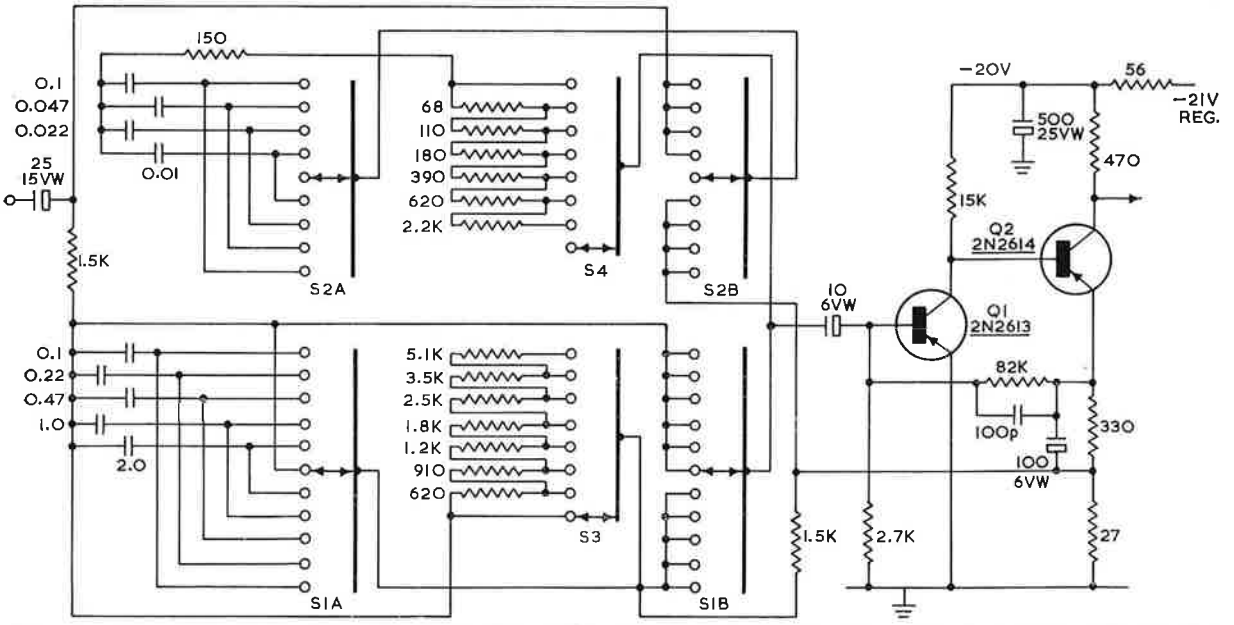


Fig. 4. Tone control section. S1, bass; S2, treble; S3, bass intensity; S4, treble intensity. All switches shown in "flat" position.

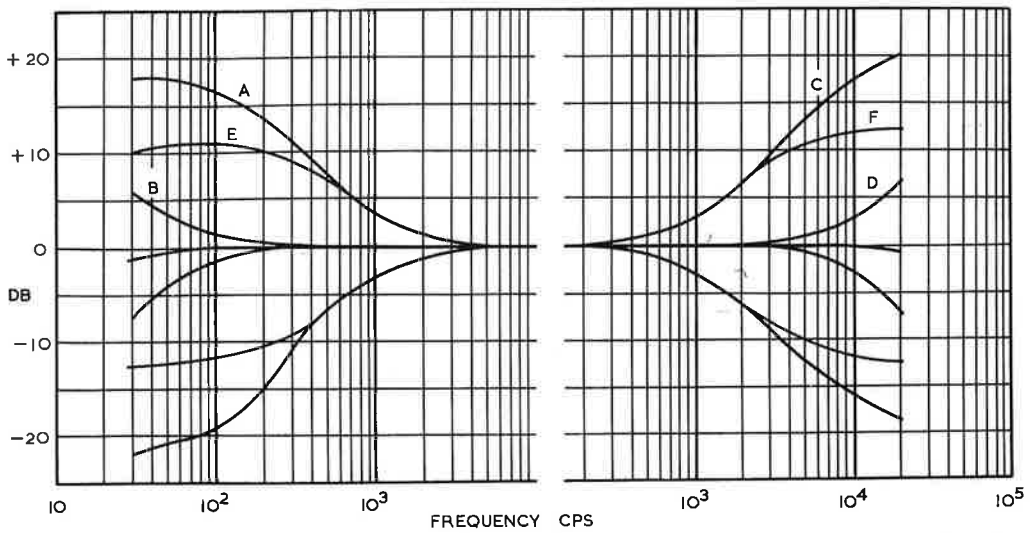


Fig. 5. Tone control response curves. A, 1 Kc/s corner frequency, maximum intensity; B, 50 c/s corner frequency, maximum intensity; C, 1 Kc/s corner frequency, maximum intensity; D, 10 Kc/s corner frequency, maximum intensity; E, 1 Kc/s corner frequency, 12dB intensity; F, 1 Kc/s corner frequency, 12dB intensity.

The balance and volume controls are connected as part of the load of Q2. Although a signal loss of 6 dB occurs due to this arrangement, the overall gain is sufficient.

Decoupling of the negative supply line to the first stage is provided by a 15,000 ohm resistor and two capacitors (25 μF, 25 VW and 0.22 μF). This filter reduces the noise from the supply line.

Ceramic Input Circuit: The circuit for use with a ceramic pickup (fig. 3) is designed using the same principles as the previously described circuit. It also uses three transistors, two A.W.V. 2N2613 and an R.C.A. 40233. The current through Q1 is once again 50 μA (approximately) for the same reasons as previously described.

The fact that the ceramic cartridge has a capacitive source impedance introduces a different problem to that of the magnetic cartridge. The impedance of the cartridge decreases as frequency increases, this causes the output current from the cartridge to increase with frequency. To obtain a flat frequency response at the output of the module, a capacitive feedback loop is provided from the emitter of Q2 to the base of Q1 by a 0.0056 μF capacitor in parallel with a 2.2M ohm resistor.

An emitter follower stage Q3 is used in both circuits to provide a low impedance to the following tone control module. It may be omitted if use is made of a tone control circuit which is satisfactory when preceded by a source of relatively high impedance.

TONE CONTROL CIRCUIT.

Tone Control Circuit: In the arrangement described here adjustment to the frequency response is obtained by switching of R-C networks in the input and feedback circuit. The required corner frequency being selected by the appropriate frequency switch (bass or treble). The mode of operation of the corner frequency (boost or cut) is determined by the relative position of the particular frequency switch. The bass frequency switch provides five positions for boost and five positions for cut, as well as a flat position. These positions correspond to corner frequencies of 1,000, 500, 200, 100 and 50 cycles per second. At these points boost or attenuation is applied at a rate approaching 6 dB per octave. Similarly the treble frequency switch provides four positions for boost and cut as well as a flat position. The corner frequencies are thus provided at 1K, 2K, 5K and 10K c/s.

Each frequency switch is operated in conjunction with an "intensity" switch. The function of this switch is to provide adjustment to the amount of boost or cut which occurs from any selected corner frequency. The maximum intensity available (boost or cut) is 21 dB.

In the bass cut position, the input signal passes through an R-C network which determines the corner frequency at which attenuation of the lower frequencies begins. The attenuation continues at a rate approaching 6 dB per octave until the maximum cut is obtained. The attenuation is controlled by the intensity switch, S3, which varies the resistance in parallel with the capacitor in the R-C network. In this bass cut position the feedback from the emitter of Q2 is

applied through a 1,500 ohm resistor to the base of Q1 and is unaffected by any frequency selective networks.

Note. The impedance at the base of Q1 is reduced to a very low value by the feedback from the emitter of Q2. It may, therefore, be neglected in the calculation of any of the corner frequencies.

When the circuit is adjusted for bass boost, the input signal passes through a 1,500 ohm resistor and then directly to the base of Q1 via the frequency switch Slb. The feedback on the other hand, is passed through an R.C. network by the switch S1a, which attenuates the low frequency components of the feedback. The gain is therefore increased at the low frequencies. Once again the corner frequency is selected by S1a and the intensity controlled by the bass intensity switch S3.

To obtain treble cut the input signal is fed through the 1500 ohm resistor and S1 directly to the base of Q1. At the same time the feedback from the emitter of Q2 passes through S2, then through the capacitor to the base of Q1. A resistive element is applied in parallel with the capacitor, via S1. This results in a parallel R-C network which reduces the gain at all frequencies below the corner frequency by a constant amount, while above the corner frequency the feedback is increased. The gain will therefore be reduced at high frequencies. The amount of attenuation or cut which will be applied is determined by the intensity switch again the maximum value being 21 dB.

In the treble boost position the input signal passes through the parallel R-C combination, selected by S2, to the base of Q1. This R-C network attenuates the signal at all frequencies below the corner frequency, while above the corner frequency the attenuation reduces at the normal rate approaching 6 dB per octave. The feedback is flat and applied through a 1,500 ohm resistor to the base of Q1 through switch S1. The amount of boost is again controlled by the intensity switch and operates as explained previously. Frequency response curves for both bass and treble are given in fig. 5.

The voltage gain of the tone control circuit is unity from the input to the emitter of Q2, with the controls in the flat position. If an input signal of 15 millivolts is applied, then the emitter signal voltage of Q2 is also 15 millivolts. The current from the collector of Q2 will be $\frac{e_s}{R_E}$,

where e_s is the signal voltage, R_E is the emitter resistance of Q2 and i_c is the a.c. signal component of the collector current

$$\therefore i_c = \frac{e_s}{R_E}$$

$$= \frac{15}{27}$$

$$= 0.65 \text{ mA}$$

The output voltage from the collector of Q2 will then be dependant on the load impedance. That is the output voltage is $i_c R_L$ where R_L is the equivalent resistance of the 470 ohm collector resistor and the external load in parallel.

The total harmonic distortion of the output current is very low due to the large amount of negative feedback from the emitter of Q2. With an input voltage of 15 millivolts the distortion is less than 0.04% total. At the same input level the signal to noise ratio is better than 47 dB unweighted and 78 dB weighted according to curve A.

References.

Hunter—Handbook of Semiconductor Electronics—(2nd Ed.). McGraw Hill, New York—Ch. 11-83.

Schwartz, M.—Information Transmission, Modulation and Noise—McGraw Hill, New York—P.197.

Simpson and Richards—Junction Transistors—Oxford, London,—P.221.

Transistor Power Supply No. 3

E. M. Woodford

This power supply was originally intended to give a fixed direct output voltage, with a low ripple content, to provide power for transistorised preamplifiers. It proved to be so successful that it was decided to increase the current rating and make the output voltage variable. The result is a versatile power supply which readers may find useful in the workshop.

The output voltage of the power supply is stabilised and adjustable from 6·5 volts to 20 volts. The maximum current available, at the full output voltage, is 150 milliamps. This current may be increased to 300 milliamps at 6·5 volts output.

CIRCUIT DESCRIPTION

The circuit uses a filament transformer which has two 6·3 volt windings connected in series. When no load is applied the voltage across the windings is 14·5 volts R.M.S. Using two A.W.V. 1N3193 silicon diodes, in a full wave voltage doubler circuit, an unregulated output of 40 volts d.c. is obtained. A reservoir capacitor of 1,000 μF is connected across the output of the voltage doubler circuit.

The regulator section of the power supply consists of three parts: a series transistor, a long-tailed pair or differential amplifier and a zener diode to provide a reference voltage.

The zener diode provides the reference voltage for the base of Q1, of the long-tailed pair and R5 is chosen to give the same voltage at the base of Q2. Any difference between the two bases, resulting from a change in the load, represents an error voltage which is amplified and appears at the collector of Q2. Thus the base voltage of Q3 alters changing the current through this transistor to compensate for changes in the load current. The output voltage therefore returns to its original value.

An alternative way of looking at the operation of this circuit is to consider the change of bias at the base of Q3 as causing a change in collector to emitter characteristics of Q3. Thus the collector to emitter voltage is altered to compensate for changes in the output voltage. In this way the output voltage is maintained essentially constant.

The 2N2869 used in the regulator circuit, since it treats the ripple voltage as a variation in the output voltage, serves as a dynamic filter and reduces the ripple voltage to a low value. Extra filtering is supplied by a 100 μF capacitor connected from the base of the 2N2869 to the positive line of the supply. The remaining ripple voltage is less than one millivolt.

DESIGN PROCEDURE

The procedure adopted in designing this power supply consisted of three major steps. The first step concerns the specifications, the second step deals with the selection of the fundamental circuit and the third step involves the calculation of the values of the various circuit components.

Step 1. Specifications. The specifications given for this supply called for a regulated output voltage

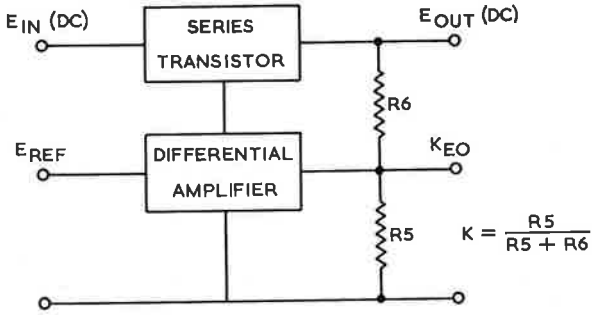
of approximately 15 volts d.c. at a current of 10 milliamps. It was essential that the ripple voltage be kept as low as possible.

In order to provide a margin on the specifications the design figures were increased to give an output voltage of 20 volts d.c. and an output current of 50 milliamps. In the finished design it was found possible to supply a load of 150 milliamps at 20 volts.

Step 2. Selection of the Fundamental Circuit. A filament transformer having two 6·3 volt windings was used to supply approximately 14·5 volts r.m.s. with no load applied.

This was followed by a full wave voltage doubler circuit to provide a d.c. voltage of approximately 40 volts to the regulator section. The size of the two capacitors in the circuit was made small, in comparison to their usual capacity, to degrade the regulation of the circuit. Thus when the load is connected the output voltage, to the regulator section of the power supply, would be expected to fall to approximately 30 volts d.c. This assists in protecting the power supply from damage which could otherwise occur from an overload or short circuit.

The regulator section of the power supply uses a differential amplifier, a series transistor and a zener diode. These were chosen because of their simplicity and reliability.



The circuit is arranged so that the difference between the voltage at $E_{(ref)}$ and the voltage at K_{EO} is as small as possible. K_{EO} being a sample of the output voltage E_{out}.

Therefore $$K_{EO} \simeq E_{(ref)}$$

i.e. $$E_{out} = (E_{ref})\left(1+\frac{R_6}{R_5}\right).$$

Since $E_{(ref)}$ is constant the output voltage may be made variable by making R_6 adjustable. The minimum output voltage will be determined by the zener diode used to provide $E_{(ref)}$. If the minimum output voltage (E_{out}) is made 6·5 volts d.c. then a zener diode of 6·5 volts nominal must be used.

Step 3. Selection of Series Transistor and Other Circuit Elements.

(*a*) Series Transistor. To decide the most suitable transistor to operate as the series element of the circuit, the maximum power which it will have to dissipate must be calculated. The maximum power dissipated by the collector (P_C) normally occurs when the output voltage is adjusted to its minimum value.

i.e. $$P_C = I_{C(max)}[E_{in(D.C.)} - E_{out(min)}]$$
$$= 0{\cdot}05(30-6{\cdot}8)$$
$$= 1{\cdot}16 \text{ watts.}$$

A medium power transistor such as an A.W.V. AS128 would overheat when dissipating this power, so that a type with a lower thermal resistance must be chosen. An A.W.V. 2N2869 with a thermal resistance of 1·5°C per watt (junction to case) was selected.

(*b*) Power Transistor and Resistances. The 2N2869 has a minimum h_{FE} of 50 at 1 amp collector current, but to provide greater latitude an h_{FE} of 40 was used in the calculations.

Thus if the output current (I_{out}) is 50 mA then the base current (I_B) will be

$$I_B(2N2869) = \frac{I_{(out)}}{h_{FE}}$$
$$= \frac{50}{40}$$
$$= 1{\cdot}25 \text{ mA.}$$

The bias resistor of the 2N2869 will have to permit a current of 1·25 milliamps when $E_{(in)} = 30V$ and $E_{(out)} = 20$ volts and $E_B \doteq E_O$.

$$\therefore R_4 = \frac{E_{(in)} - E_{(out)}}{I_B}$$
$$= \frac{30-20}{1{\cdot}25\times10^{-3}}$$
$$= 8\times10^3 \text{ ohms}$$

The bias resistor of the 2N2869 will be 8·2K ohms.

(*c*) Differential Amplifier. The maximum current which can be expected to flow in the bias resistor of the 2N2869 may be found from

$$I_{B(max)} = \frac{E_{(in)} - E_{(out)\,min}}{R}$$
$$= \frac{40-6{\cdot}8}{8{\cdot}2\times10^3}$$
$$= 4 \text{ mA approx.}$$

If little or no output current is required then this 4 milliamps of current must be taken by the collector of Q2 in the differential amplifier, to prevent the output voltage from rising. To do this the collector current of this transistor will have to be permitted to vary between zero and 4+2·8 milliamps (I_{CBO} of 2N2869 <2·8 mA at 50°C). The

latter occurring at zero output current and minimum output voltage.

The differential amplifier also contains a common emitter resistor which determines the total current taken by the differential pair in the active region. Since the zener diode holds the base of Q1 at 6·8 volts then the emitter voltage of the two transistors will be approximately 6·65 volts. Therefore, if the collector current of the second transistor is to vary by 6·8 milliamps, the current through the emitter resistor must be at least 6·8 milliamps. If a small safety margin is again provided and an emitter current of 8 milliamps chosen for the pair, then the emitter resistor

$$R_3 = \frac{E_E}{I_E}$$
$$= \frac{6{\cdot}65}{8\times10^{-3}}$$
$$= 830 \text{ ohms.}$$

The emitter resistor therefore will be 820 ohms.

The next problem is the provision of a current to operate the zener diode. For the zener diode to operate in its zener region and independently of the base current of Q1, the current provided should be greater than the maximum base current which can be expected to flow in Q1.

Assuming that Q1 has a minimum h_{FE} of 60, then the base current (I_B) may be determined.

$$I_{B\,(Q1)} = \frac{I_C}{h_{FE}}$$
$$= \frac{8{\cdot}0\times10^{-3}}{60}$$
$$= 0{\cdot}13 \text{ mA.}$$

Therefore a current of 5 milliamps would be sufficient to swamp the base current of Q1 and cause the zener diode to operate always in its zener mode. Using $E_{(in)}$ as the supply voltage the required resistance may be calculated.

$$R_1 = \frac{E_{(in)} - E \text{ zener}}{I}$$
$$= \frac{30-6{\cdot}8}{5\times10^{-3}}$$
$$= 4{\cdot}65K \text{ or } 4{\cdot}7K \text{ ohms.}$$

To determine the value of $R5$ and $R6$ a similar procedure is adopted to that used in calculating $R1$. A small current is selected to flow through the divider, but it must be large enough to swamp the base current of Q2. The base current will be approximately the same value as for Q1, that is 0·13 milliamps. If a current of 1·5 milliamps is chosen then the value of $R5$ may be calculated. It must be remembered that the base of Q2 will be held at 6·8 volts by the action of the zener diode on the base of Q1. Therefore

$$R_5 = \frac{6{\cdot}8}{1{\cdot}5\times10^{-3}}$$
$$= 4{,}500 \text{ ohms.}$$

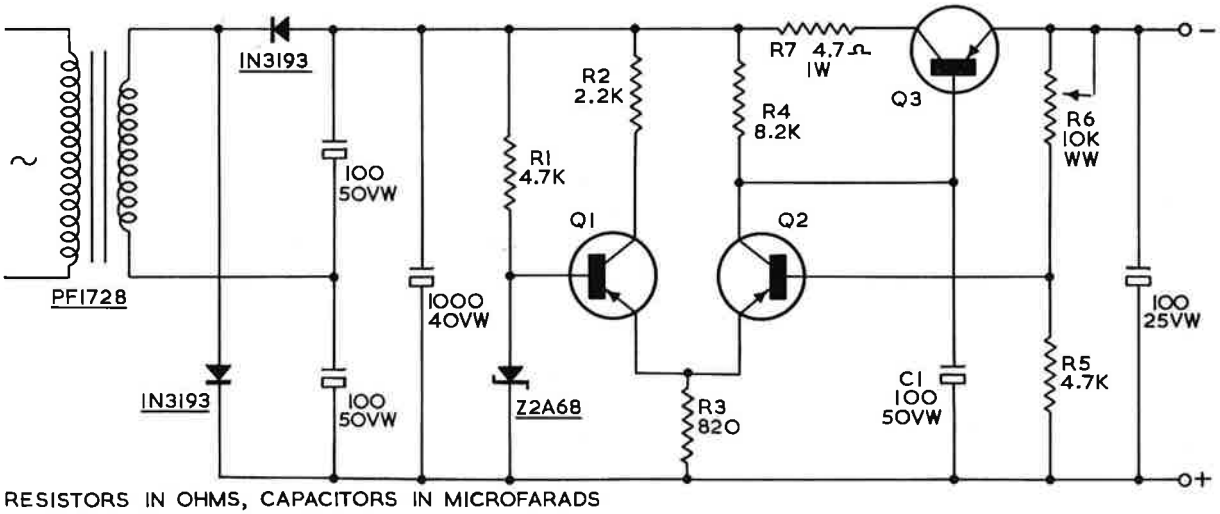
i.e. $4{\cdot}7K$ ohms.

Similarly R_6 may be calculated

$$R_6 = \frac{E_{out\,(max)} - E_{B\,(Q2)}}{I}$$
$$= \frac{20-6{\cdot}8}{1{\cdot}5\times10^{-3}}$$
$$= 8{\cdot}8K \text{ ohms.}$$

Alternatively, as mentioned previously,

$$\frac{R_6}{R_5} = \frac{E_{(out)} - E_{(ref)}}{E_{(ref)}}$$



RESISTORS IN OHMS, CAPACITORS IN MICROFARADS

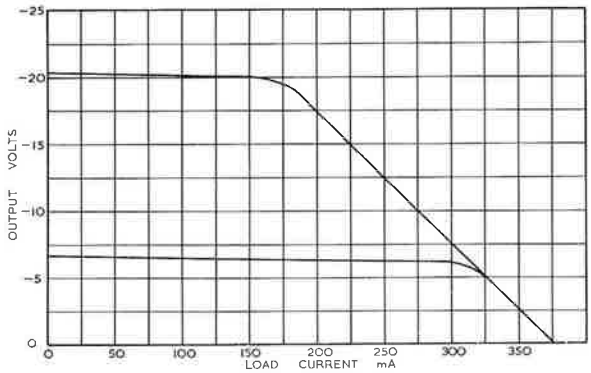
Circuit diagram of the transistor power supply.

i.e. $$R_6 = R_5\left(\frac{E_{(out)} - E_{(ref)}}{E_{(ref)}}\right)$$

$$= 4{,}500\left(\frac{20-6{\cdot}8}{6{\cdot}8}\right)$$

$$= 8{\cdot}8K \text{ ohms.}$$

The potientometer chosen was the nearest standard value, being $10K$ ohms. It is advisable to use a wire wound potientometer in this position, due to the d.c. current flowing through the divider.



Regulation characteristics — output voltage versus load current.

The two remaining resistors, R_2 and R_7, are both current limiting devices. R_2 is included to prevent excess current causing damage to the zener diode, should Q1 be accidentally shorted. R_7 reduces the maximum current flow through Q3 should the output voltage be shorted. This prevents damage to the 2N2869.

The capacitor C_1 is chosen to present a low impedance, at the base of Q3, to the ripple frequency of 100 cycles per second. It is necessary for the base of Q3 to be held steady so that the regulator transistor, by feedback action, can neutralise the ripple voltage appearing at the output.

Another capacitor (C2) is placed across the output, in parallel with the load, to assist in the regulation of the output voltage. It reduces small variations in the output voltage due to changes in the load conditions, by providing a reservoir action, due to its stored charge.

At this point the power supply was constructed and the voltages around the circuit measured. In this way measurements of the exact operating conditions permitted more accurate calculations of the thermal conditions.

With no load applied and the output voltage control set at its maximum point, the output voltage was 27 volts. The input voltage to the differential amplifier (E_{in}) was 42 volts. When a load was applied E_{in} fell and continued to fall as the load current was increased. With a short circuit applied to the output E_{in} fell to 16·5 volts. When the mains supply was increased by 10 per cent E_{in} rose to 44 volts d.c. and the short circuit current increased to 420 milliamps.

These measurements enabled the thermal characteristics of the power supply to be determined with reasonable accuracy. The first step is to calculate the required junction to ambient thermal resistance ($R\theta_{J-A}$) to allow safe operation at the maximum ambient temperature at which the power supply will be expected to operate. If this temperature is taken as 50°C then the required thermal resistance from the junction to air ($R\theta_{J-A}$) may be determined. From the specifications of a 2N2869 it is found that the maximum junction temperature ($T_{J\,(max)}$) is 100°C, and the junction to case thermal resistance ($R\theta_{J-C}$) of 1·5°C per watt maximum. This calculation must be made assuming a combination of all the worst conditions, that is with the maximum ambient temperature (T_A), with a short circuit load condition and with a ten per cent increase in mains supply voltage. Under these conditions the collector power of Q3 is

$$P_{C\,(Q3)} = I_{C\,(max)}(E_{in} - E_{out})$$
$$= 0{\cdot}42(44-26)$$
$$= 7{\cdot}75 \text{ watts.}$$

But $$R\theta_{J-case} = 1{\cdot}5°\text{C/watt.}$$

$$\therefore\ R\theta_{case-A} = R\theta_{J-A} - R\theta_{J-case}$$
$$= 6{\cdot}45 - 1{\cdot}5$$
$$= 4{\cdot}95°\text{C/watt.}$$

Note: $R\theta_{case-A}$ includes $R\theta_{case-fin}$.

Therefore $$R\theta_{J-A} = \frac{T_{J\,(max)} - T_{A\,(max)}}{P_C}$$

$$= \frac{100-50}{7{\cdot}75}$$

$$= 6{\cdot}45°\text{C/watt.}$$

This figure indicates the use of a reasonably small heat sink such as a Ferris $4'' \times 2''$ anodised aluminium sink. However the conditions used to determine this figure are a combination of all the worst conditions acting simultaneously. Since in actual practice it is most unlikely that all these conditions will occur together, it may be possible to use a smaller heat sink. However this will depend on the user and the actual operating conditions.

CONSTRUCTION

The construction of the power supply is simple and offers no problems. Any suitable layout may be used providing the heat sink for the 2N2869 is large enough and is given sufficient ventilation. The 2N2869 should be mounted on the heat sink using silicon grease, a lead washer and a mica washer.

ACKNOWLEDGMENT

The author wishes to acknowledge the valuable assistance given by Mr. D. K. Money who designed the original circuit.

Achieving High Performance in VHF/UHF Tuned Amplifiers

T. J. ROBE *

When stable power gain and low noise figure are performance objectives in the design of RF amplifiers, the selection of transistors and component values are critical. The author develops the principles of design for these circuits with a design example.

IF YOU think that gain can be traded for bandwidth in transistorized RF amplifiers, you are mistaken. A close look at the design of these important networks reveals that over a large range of possible bandwidths the gain will remain constant.

The reasons for this situation are apparent only after a careful analysis of the circuit.

The most significant characteristics of a high-performance RF transistor amplifier are noise figure for low signal levels and power gain and stability at the operating frequency. The type of transistor used determines the noise figure and the amount of power gain at the operating frequency. The circuit configuration affects both stability and power gain, and the no-signal bias point influences both power gain and noise figure. Thus, the proper selection of the transistor, the configuration and the operating point are the important factors in the design of an RF amplifier.

TRANSISTOR CHOICE AFFECTS GAIN AND NOISE FIGURE

The design of the amplifier starts with the choice of the transistor. Maximum ratings are determined from the manufacturer's data sheets. Once these are considered, an estimate of stable gain and noise figure can be made.

The figure of merit most useful in making a quick comparison between the relative power-gain capability of various transistors is f_{max}, the frequency at which the maximum available power gain (MAG) is unity (0 db). This frequency can be calculated from:

$$f_{max} = \left(\frac{f_t}{25\, r_{bb}'\, C_c}\right)^{1/2} \qquad (1)$$

where f_t is the gain-bandwidth product and $r_{bb}' C_c$ is the collector-to-base time constant.

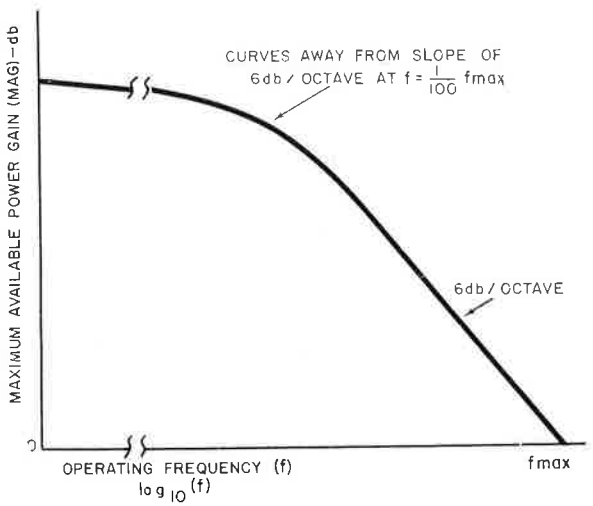


Fig. 1. Maximum available power gain as a function of operating frequency for an RF transistor. Note that the gain falls at a rate of 6 db per octave up to f_{max} when it is equal to 0 db.

*Radio Corporation of America, Electronic Components and Devices, Somerville, N.J.

Recent UHF transistors, such as the 2N2857, have typical values for f_{max} of 2·25 Gc. Below f_{max}, MAG varies as shown in Fig. 1. For a given frequency, f, in the minus 6-db-per-octave region, MAG can be approximated by the following expression:

$$\text{MAG (in db)} = 20 \log_{10} \frac{f_{max}}{f} \qquad (2)$$

The exact expression for MAG is given by the transistor-admittance parameters:[1]

$$\text{MAG} = \frac{Y_{21}}{4\, Y_{11}\,(real)\; Y_{22}\,(real)} \qquad (3)$$

This gain, useful for comparison, can seldom be achieved in practical circuits, because it is based on the assumption that no feedback exists in the circuit. The maximum stable usable gain (MUG) per stage that can be achieved in a multistage common-emitter circuit is given by the following expression:

$$\text{MUG (in db)} = 10 \log_{10} \frac{2K\, Y_{21}}{\omega C_{fb}} \qquad (4)$$

where K is an arbitrary skew factor that should not exceed 0·4 for fixed-gain stages or 0·2 for automatic-gain-controlled stages;[2] Y_{21} is the magnitude of the transistor forward transadmittance, and C_{fb} is the total circuit feedback capacitance from collector to base. With Eq. 4, the maximum stable un-neutralized power gain can be estimated if C_{fb} is made equal to the C_{ob} of the transistor. When four-lead isolated-collector transistors are used, care must be taken to choose the data-sheet C_{ob} value with the fourth lead (case) grounded. In practice this lead should be connected to signal ground to reduce the over-all feedback capacitance. As an example, C_{ob} for the 2N2857 is approximately 0·8 pf with the case grounded, which represents a decrease of 0·5 pf from the C_{ob} value with the fourth lead open. The important transistor parameters for power gain, therefore, are high f_t, low $r_{bb}{}' C_c$, and low C_{ob}. In addition to these data, the manufacturer usually specifies a minimum expected power gain (MAG or MUG) when the transistor is used in a specific functional circuit at a frequency within the specified frequency range. Eq. 3 indicates that transistors having either a high $|Y_{21}|$ or low Y_{22} (real) would give a high MAG. It is preferable, however, that the transistor have a high Y_{21} rather than a very low Y_{22} (real). The reason is that the desired selectivity and the minimum parallel capacitance that can be obtained in the output tank circuit place a lower limit on the value of the transistor output conductance which can be matched for maximum power gain.

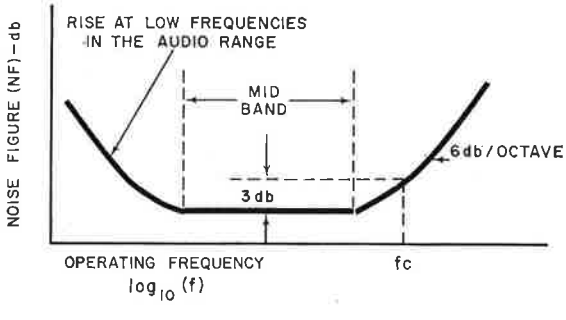


Fig. 2. Noise figure as a function of operating frequency for an RF transistor. When the operating frequency approaches the alpha cut off frequency, the noise figure rises at 6 db per octave. At f_c the noise figure is 3 db above the midband value.

Noise-performance comparisons are more difficult to evaluate accurately, because transistor noise figure varies considerably with bias conditions and source impedance. Usually the manufacturer will specify a maximum noise figure for a functional circuit at optimum transistor bias conditions and source resistance. The specified source resistance appears at the transistor's input terminals. It includes the effects of any transformations between the generator and the transistor. Neilsen[3] has derived the following expression, from which an estimate within 1 db of the noise figure at other than the manufacturer's test conditions can be calculated:

$$\text{NF} = 1 + \frac{r_{bb}{}'}{R_g} + \frac{r_e}{2R_g} + \frac{(R_g + r_{bb}{}' + r_e)}{2R_g r_e h_{feo}} \left[1 + \left(\frac{f}{f_a} \right)^2 (1 + h_{feo}) \right] \qquad (5)$$

As an example, the following calculation can be made for the 2N2857 transistor at $f = 450$ Mc, $V_{CE} = 6$ v, $I_C = 1{\cdot}5$ ma, $R_g = 50$ ohms, and $f\alpha$ (the alpha-cutoff frequency) = 1·1 Gc:

$$\text{NF} = 1 + \frac{15}{50} + \frac{17}{100} + 0{\cdot}039 \left[1 + \frac{0{\cdot}45^2}{1{\cdot}1} (100) \right] = 2{\cdot}13$$

This figure is equivalent to 3·3 db; a typical measured value is 4·0 db.

The terms in Eq. 5 that most likely will differ from the manufacturer's test data are: $r_e = 26/I_e$ (ma) ohms; R_g, the source resistance; h_{feo}, the low-frequency value of h_{fe}; and f, the frequency of operation. Eq. 5 shows that when the frequency makes the term $(f/f\alpha)^2(1+h_{feo})$ much less than 1, the noise figure is independent of frequency. When this term is not small compared with 1, the noise figure increases as the frequency increases, and it approaches a positive slope of 6 db per octave, as shown in Fig. 2.

The upper-noise-corner frequency, f_c, is defined as the frequency at which the noise figure is 3 db higher than the midband value. This frequency,

determined by manipulation of the last term in Neilsen's equation, is given approximately by[4]

$$f_c \approx f_\alpha \left[\frac{r_e(2R_g + 2r_{bb}' + r_e)}{R_g + r_e + r_{bb}'} \right]^{\frac{1}{2}} \qquad (6)$$

For the 2N28527 transistor with $R_g = 50$ ohms and $I_c = 1{\cdot}5$ ma, a typical mid-frequency noise figure is 3 db, and f_c is approximately 700 Mc.

If R_g is 400 ohms and I_c is one ma, the mid-band NF is typically 2 db. Eq. 5 shows that the important transistor parameter requirements for good high-frequency noise performance are low r_{bb}', high h_{feo}, and high $f\alpha$, which are the requirements for maximum power gain.

TRANSISTOR CONFIGURATION INFLUENCES POWER GAIN AND STABILITY

The noise figure mostly depends on the type of transistor used in the front-end stage. The least noise contributed by succeeding stages, however, depends on the configuration that provides the most power gain. Maximum power gain is obtained with the common-emitter configuration, provided the frequency of operation is well below the f_t of the transistor. Additional advantages of common-emitter operation are:

- The optimum noise-source resistance is closest to the optimum source resistance for best power gain.
- The frequency range of unconditional stability is wider than for the commonbase configuration.

Common-base operation has certain advantages over common-emitter operation. These are:

- Operating frequencies can be much higher than allowable with the common-emitter configuration before neutralization is required.
- At frequencies approaching the f_t of the transistor, the common-base configuration generally offers higher power gain than the common-emitter, when both are operated unneutralized.
- Power gain is least affected by changes in transistor parameters, such as might be the case when a transistor is replaced.

The common-collector configuration is not normally used as an RF amplifier, because it has an extremely narrow range of frequencies over which it is unconditionally stable. In addition it offers the lowest power gain of the three configurations.

The choice of the no-signal bias point depends on the relative importance of noise, power gain and agc performance. Front-end stages should be biased for best noise performance with reasonable power gain; intermediate stages should be biased for best power gain and agc performance. Fig. 3 shows the variation of $|Y_{21}|$ with collector current. This results in a change in MUG as a function of collector current, as shown in Eq. 4. Fig. 3 indicates that reverse agc could be applied with quiescent bias currents up to about 4 ma. Eq. 4 also shows that a reduction of transistor feedback capacitance, the result of an increase in collector voltage, will also increase the MUG.

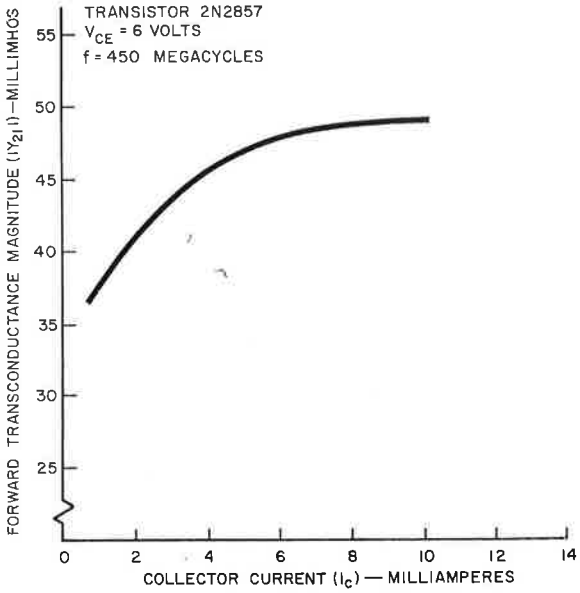


Fig. 3. The average forward transadmittance magnitude as a function of operating collector current for a 2N2857 transistor. Measurements were made at 450 Mc with V^{CE} equal to 6 v.

From a noise standpoint, Eq. 5 has several parameters that are bias-dependent. These are r_e, $f\alpha$ and h_{feo}. To determine the optimum low-noise bias, it is easier to make a series of noise-figure measurements as a function of collector current and voltage than to determine values for the varying parameters and to solve the noise-figure equation at each bias point. The transistor manufacturer normally specifies an optimum bias, determined by a functional noise-figure test. For the 2N2857, this bias is $I_C = 1{\cdot}5$ ma and $V_{ce} = 6$ v.

BASIC RELATIONSHIPS ENSURE STABLE NETWORK DESIGN

RF circuit design involves the following three steps: the calculation of MAG, the calculation of MUG for a given degree of neutralization and stability, and the design of interstage circuitry necessary to achieve the calculated MUG. An attempt to achieve MAG solely by neutralization is impractical, because the feedback term, Y_{12}, varies from transistor to transistor and with temperature,

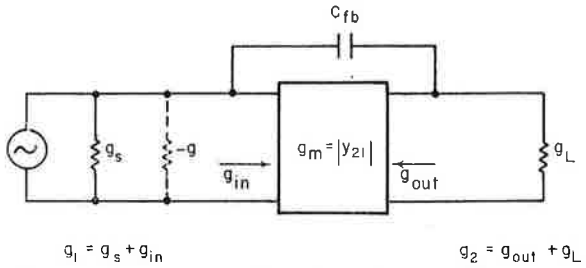


Fig. 4. Common-emitter tuned amplifier stage showing the important parameters required for deriving Eqs. 7 through 9.

bias and frequency. An attempt to stabilize by mismatch reduces gain excessively. This is especially true with the common-emitter configuration where the feedback capacitance is greater than that for the common-base configuration. A combination of mismatch and neutralization is desirable.

In the common-emitter tuned amplifier stage in Fig. 4, with feedback capacitance C_{fb}, it can be shown[5] that at frequencies below resonance the maximum negative conductance $(-g)$ reflected across the input terminals is given by

$$-g = \frac{g_m w C_{fb}}{2g_2} \tag{7}$$

where $g_2 = g_{out} + g_L = (1+m)g_{out}$. The quantity m = mismatch ratio $= g_s/g_{in} = g_L/g_{out}$.

If C_{fb} is sufficiently large, so that $-g$ equals g_1, where $g_1 = g_{in} + g_s$, the amplifier will oscillate. The quantity g_1 also equals $(1+m)g_{in}$. The limiting value of C_{fb} to prevent oscillation is given by

$$C_{fb\,max} = \frac{2g_1 g_2}{\omega g_m} \tag{8}$$

Actually, however, the value of C_{fb} should be sufficiently lower than $C_{fb\,max}$ to prevent objectionable skewing of the response curve. The actual allowable C_{fb} is given by

$$C_{fb} \leqslant KC_{fb\,max} \leqslant \frac{2Kg_1 g_2}{\omega g_m} \tag{9}$$

where K is the arbitrary skew factor. Because stability is ensured when Eq. 9 is satisfied, the designer has a choice of reducing C_{fb} by neutralization or raising the $g_1 g_2$ product by mismatching.

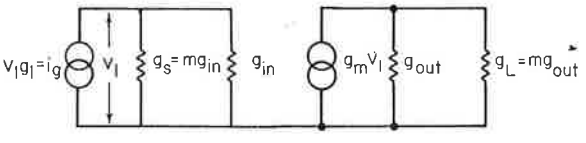


Fig. 5. The equivalent circuit of Fig. 4 with input and output sections isolated from one another. This configuration is used to derive Eq. 10.

With regard to stability requirements, consider a single-stage amplifier with equal mismatch ratio at input and output ($m = g_s/g_{in} = g_L/g_{out}$) and the susceptance component at each terminal tuned out. The general expression for transistor power gain G_P is:

$$G_P = \frac{\textit{power delivered to load}}{\textit{maximum available power from source}}$$

Fig. 5 is the circuit of Fig. 4 redrawn, but with the input and output sections isolated from one another. By substitution of the appropriate values from Fig. 5, the equation for gain becomes

$$G_P = \frac{16m^2}{(1+m)^4}\text{MAG} \tag{10}$$

Eq. 10 assumes adequate mismatch so that the effects of mismatch are negligible.
From Eqs. 3 and 9, the condition required to ensure stability is

$$\frac{2Kg_m}{\omega C_{fb}} = \frac{4}{(1+m)^2}\text{MAG} \tag{11}$$

The mismatch ratio m required for a given skew factor K and feedback capacitance C_{fb} can be calculated from Eq. 11. This ratio can then be used in Eq. 10 to determine the MUG of the single-stage amplifier.

For design objectives other than power gain, it may not be desirable to mismatch both terminals of the transistor equally. If a primary consideration is low-noise performance, it is usually necessary to present a fixed optimum value of source conductance to the transistor input, thereby fixing the input ratio. The output mismatch will then have to be adjusted so that the $g_1 g_2$ product satisfies Eq. 9. When unequal mismatch conditions exist, Eqs. 10 and 11 become, respectively:

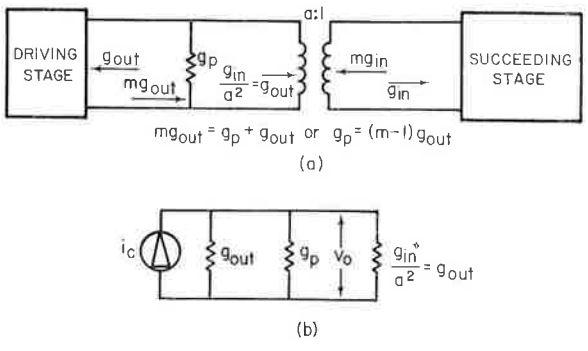


Fig. 6. Common emitter multistage amplifier configuration (a) showing interstage network parameters and (b) equivalent circuit for the derivation of Eqs. 14, 15 and 16.

$$G_P = \frac{4m_1}{(1+m_1)^2} \cdot \frac{4m_2}{(1+m_2)^2}\text{MAG} \qquad (12)$$

and

$$\frac{2Kg_m}{\omega C_{fb}} = \frac{2}{(1+m_1)} \cdot \frac{2}{(1+m_2)}\text{MAG} \qquad (13)$$

where m_1 is the input mismatch and m_2 the output mismatch.

For multi-stage amplifiers, realization of the optimum mismatch condition (input and output equally mismatched) necessitates the addition of an external loss, g_p, by use of either a low-Q coil or a resistor in parallel with the tuned tank. Fig. 6 shows the schematic and equivalent circuit for the analysis.

The mismatch loss, L, is equal to the power delivered to the succeeding stage divided by the power available from the driving stage:

$$L = \frac{4}{(1+m)^2}$$

The loss factor multiplied by the stage MAG gives the MUG attainable per stage:

$$\text{MUG} = \frac{4}{(1+m)^2}\text{MAG} \qquad (14)$$

From Eq. 11, MUG can be written as

$$\text{MUG} = \frac{2Kg_m}{\omega C_{fb}} \qquad (15)$$

The loss component, g_p, can be calculated from the relationship

$$g_p = (m-1)g_{out} \qquad (16)$$

Calculations of the mismatch ratio, MUG, and MAG can be made with Eqs. 11, 15 and Eqs. 2 or 3, respectively.

The effect of cascading stages on the value of the skew factor, K, should also be considered in the design of the multi-stage common-emitter amplifier. B. J. T. Thompson[6] has shown that K should be divided by a factor of 2 for two stages, 2·61 for three stages, and 3 for four stages.

Consider now a common-base amplifier configuration. It can be shown that if a two-port network is to be stable, the following relation must hold:[7]

$$S = \frac{2(g_{11}+g_G)(g_{22}+g_L)}{|Y_{21}Y_{12}|+Y_{21}Y_{12}(\text{real})} \geq 1$$

For a well-designed amplifier, the stability figure, S, should be at least 5. If, therefore, mg_{11} is substituted for g_g and mg_{22} for g_L:

$$S = \frac{2(1+m)^2 g_{11}g_{22}}{|Y_{21}Y_{12}|+Y_{21}Y_{12}(\text{real})} \geq 1 \qquad (17)$$

The factor m can be found from Eq. 17, and Eqs. 10 or 14 can then be used to calculate the MUG.

PRACTICAL DESIGN PROCEDURE FOR RF INTERSTAGE NETWORK

Let us design an interstage network for a four-stage, 200-Mc, unneutralized common-emitter amplifier, using 2N2857 transistors at $V_C = 6$ v, $I_C = 1{\cdot}5$ ma, and $f = 200$ Mc:

$C_{ob} = 0{\cdot}8$ pf (case grounded).
$Y_{11} = Y_{ie} = 3+j6$ millimhos.
$Y_{22} = Y_{oe} = 0{\cdot}3+j2$ millimhos.
$|Y_{21}| = |g_{fe}| = 45$ millimhos.

From Eq. 2:

$$\text{MAG} = 20 \log \frac{2{\cdot}25}{0{\cdot}2} = 21 \text{ db.}$$

From Eq. 15:

MUG per stage =

$$\frac{2{\cdot}0(0{\cdot}132)(45)\times 10^{-3}}{6{\cdot}28(200\times 10^6)(0{\cdot}8\times 10^{-12})}$$

$$= 11{\cdot}9 \text{ (or 11 db)} \cdot$$

The factor 0·132 in the above equation is the product of the skew factor (0·4) and the four-stage reduction factor (0·33). From Eq. 14:

$$(1+m)^2 = \frac{4\text{ MAG}}{\text{MUG}} = \frac{4(121)}{11{\cdot}9} = 40{\cdot}5,$$

from which $m = 5{\cdot}36$.

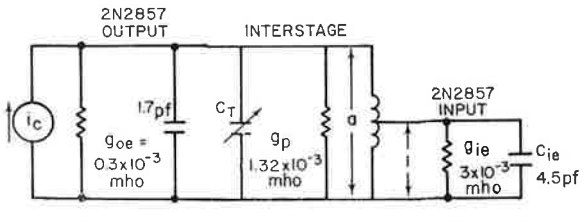


Fig. 7. Common-emitter RF amplifier circuit using 2N2857 transistors. Circuit is developed in the design example.

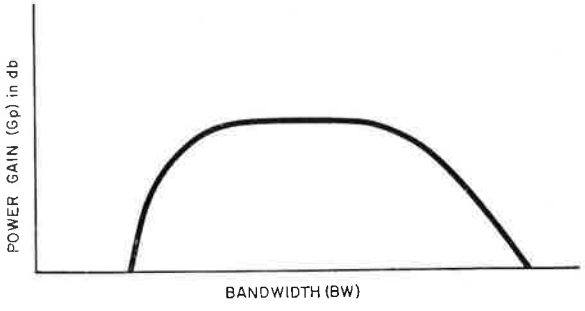


Fig. 8. Power gain as a function of bandwidth shows that power gain remains fairly constant over a wide range of bandwidths.

From Eq. 16, $g_p = 1{\cdot}32$ millimhos and, therefore, the loss-component resistor equals 750 ohms. If an operating stage Q of 10 is assumed:

$$10 = \frac{\text{total parallel tank resistance}}{\text{tank reactance}}$$

$$\frac{1}{\frac{2g_{oe}+g_p}{X_L}} = \frac{455}{X_L},$$

so that $X_L = 455/10 = 45{\cdot}5$ ohms.

Therefore, the inductance of the tank is 0·035 μh. The capacitance, which tunes with 0·035 μh at 200 Mc, is 18 pf. Because there is a parallel capacitance of about 2 pf from the transistors themselves, C_t should tune near 16 pf. The turns ratio, a, is determined from the following expression:

$$a = \left(\frac{g_{out}}{g_{in}}\right)^{1/2} = \left(\frac{3}{0{\cdot}3}\right)^{1/2} = 3{\cdot}2$$

The developed circuit is shown in Fig. 7.

Although many designers think that gain and bandwidth can be traded, the curve of power gain G_p as a function of bandwidth (Fig. 8) shows that this isn't true. For a relatively large range of bandwidths the power gain is constant[8] and is determined by Eq. 10.

The fall-off in gain at narrow bandwidths is caused by the high tank coil losses, whereas the fall-off at wide bandwidths is attributable to the addition of the external resistance necessary to obtain an operational Q lower than that of the transistor output circuit.

Additional problems with exceptionally wide bandwidths are the difficulties encountered in obtaining wideband neutralization and significant changes in transistor impedance levels over the band.

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